SNPD1730 Series
USB Type-C Port Controller

1 Introduction

1.1 Features

- Memory configuration
  – 16 KB on-chip flash programming memory
  – 1.25 KB SRAM
- 8-bit 8051 with frequency up to 8 MHz
- On-Chip Debug System (OCDS) interface
- Built-in Watchdog Timer (WDT)
- Interrupt sources including BMC, QC I/O, ADC, OVP, UVP, SCP, OCP, OTP, NDT, T0, and T1
- 5V I/O pin configuration
  – Bi-directional
  – Wakeup I/Os
  – Pull-up resistors
  – 10 mA source and sink current
- High voltage I/O pin configuration
  – Gate driver control I/O for external MOS: VBUS_CTRL
  – Sink currents for discharge and monitor: DISC_MON
  – Cathode I/O for shunt regulator: CATH
- Type-C and USB-PD support
  – USB PD 3.1 Version 1.1 specification including Programmable Power Supply (PPS) and EPR 28V modes
  – Configurable resistors R_P and R_D
  – One USB Type-C port and one Type-A port
  – VCONN power and switch for reading E-Marked cable
- Quick Charge™ (QC) protocol
  – Supports one set of QC I/O and integrates all required terminations on DP/DM lines
  – Supports BC1.2, QC 2.0/3.0/4.0/4.0+/5.0
- Shunt regulator
  – Analog regulation of secondary side feedback node (optocoupler)
  – For VBUS control with step 20 mV, 14.6 mV or 10 mV ranging from 3V to 29.4V output
  – Constant current or constant voltage mode
  – Supports low-side current sensing for constant current feedback for the optocoupler
- Operating voltage and temperature
  – 3V to 30V operation from VCC
  – Working temperature range: -40°C to 105°C
- Internal 5V regulator output
  – Power input from VCC
  – Driving current 20 mA output with external 1 µF capacitor
- Low-side Current Sense Amplifier (LSCSA)
  – Programmable gain control: 20, 40, 60, 80, and 100
  – Built-in offset cancellation
- Built-in 12-bit SAR ADC with 4-level internal reference
  – Up to two channels of ADC input
  – Internal reference voltage: 2V, 3V, 4V, and VDD
- Two 8-bit timers: T0 and T1
- 2.6V LVD for VDD
- System clocks
  – Internal high clock: RC type 32 MHz
  – Internal low clock: RC type 16 kHz
- Three operating modes
  – Normal mode: Both high and low clocks are active
  – Idle mode: Wakeup by interrupts
  – Stop mode: Wakeup by I/O, QC I/O, and CC-PHY
- Packages
  – QFN16L
  – QFN20L

1.2 Description

The SNPD1730 series is a highly integrated USB Type-C port controller that complies with the latest USB Type-C and Power Delivery (PD) standards. With Sonix's proprietary 8051 technology, the SNPD1730 series consists of an 8-bit 8051 processor, a 16 KB on-chip flash programming memory, a complete Type-C USB-PD transceiver, an integrated feedback control circuit for voltage (VBUS) regulation, and all termination resistors required for a Type-C port. Featuring multiple I/Os, well-integrated BOM, and system-level ESD protection, the SNPD1730 series is well-suited for power adapter applications.

1.3 Selection Table

Table 1–1 Selection Table

Device	BMC PHY	QC I/O	Shunt LDO	LSCSA	ADC	Timer	I/O	Package	Tape & Reel Packing
SNPD1733FJG	✓	✓	✓	✓	✓	2	2	QFN16L	–
SNPD1733FJGR[1]	✓	✓	✓	✓	✓	2	2	QFN16L	✓
SNPD17331FJG	✓	✓	✓	✓	✓	2	2	QFN16L	–
SNPD17331FJGR[1]	✓	✓	✓	✓	✓	2	2	QFN16L	✓
SNPD17332FJG	✓	✓	✓	✓	✓	2	3	QFN16L	–
SNPD17332FJGR[1]	✓	✓	✓	✓	✓	2	3	QFN16L	✓
SNPD1734HJG	✓	✓	✓	✓	✓	2	4	QFN20L	–
SNPD1734HJGR[1]	✓	✓	✓	✓	✓	2	4	QFN20L	✓

1.4 Functional Block Diagram

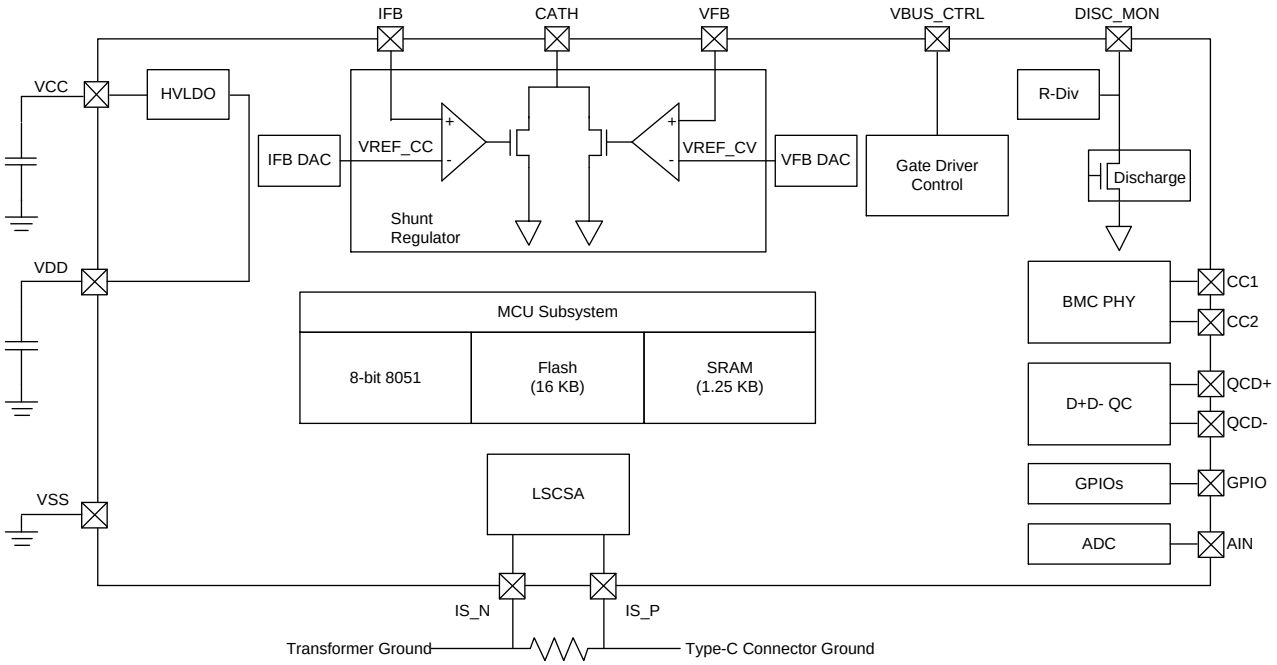

Figure 1–1 Functional Block Diagram

[1] The suffix "R" does not appear on the marking. It is for procurement purpose only.

Revision History

Date	Revision	Description
06-Mar-2023	1.0	Initial release

Convention

ⓘ **WARNING**	Indicates a hazard with a medium or low level of risk that, if not avoided, could result in minor or moderate injury.
🛠 **TIP**	Indicates a tip that may help you solve a problem or save time.
🕮 **NOTE**	Provides additional information to emphasize or supplement important points of the main text.

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2.1.1 Pin Assignment

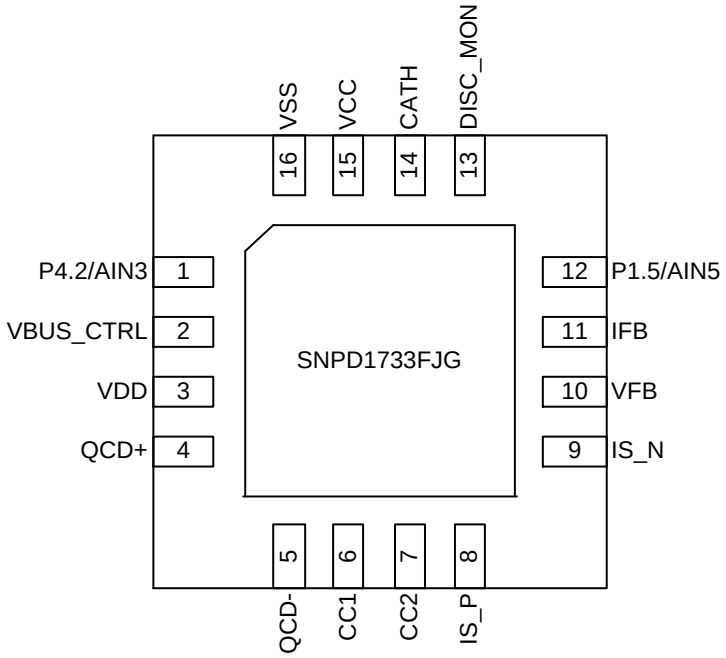


Figure 2–1 SNPD1733FJG Pin Assignment

2.1.2 Pin Description

Table 2–1 SNPD1733FJG Pin Description

Name	No.	Type[2]	Description
P4.2	1	I/O	General purpose digital input/output
AIN3		AI	ADC input channel 3
VBUS_CTRL	2	I/O	External MOSFET control
VDD	3	P	HV LDO output for digital and analog circuits
QCD+	4	I/O	USB D+ channel
QCD-	5	I/O	USB D- channel
CC1	6	I/O	Type-C connector configuration channel 1
CC2	7	I/O	Type-C connector configuration channel 2
IS_P	8	AI	Positive input of a current sense amplifier for output current sensing
IS_N	9	AI	Negative input of a current sense amplifier for output current sensing
VFB	10	AI	Feedback input for the constant-voltage loop
IFB	11	AI	Feedback input for the constant-current loop
P1.5	12	I/O	General purpose digital input/output
AIN5		AI	ADC input channel 5
DISC_MON	13	AO	Type-C VBUS monitor with internal discharge FET
CATH	14	AI	Cathode of voltage regulation and compensation for other applications
VCC	15	P	Power supply input voltage
VSS	16	GND	Power supply ground

[2] Signal Types:
I = Input
O = Output
A = Analog signal
P = Power
GND = Ground

2.2 SNPD17331FJG

2.2.1 Pin Assignment

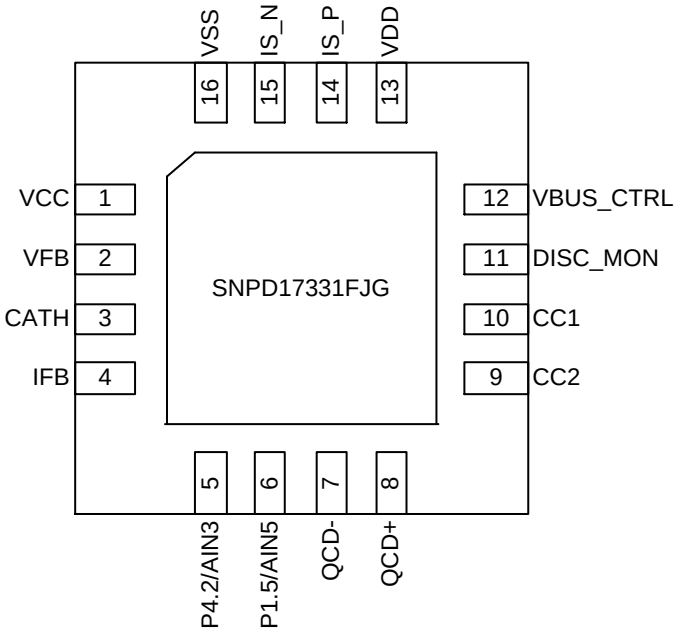


Figure 2–2 SNPD17331FJG Pin Assignment

2.2.2 Pin Description

Table 2–2 SNPD17331FJG Pin Description

Name	No.	Type[3]	Description
VCC	1	P	Power supply input voltage
VFB	2	AI	Feedback input for the constant-voltage loop
CATH	3	AI	Cathode of voltage regulation and compensation for other applications
IFB	4	AI	Feedback input for the constant-current loop
P4.2	5	I/O	General purpose digital input/output
AIN3		AI	ADC input channel 3
P1.5	6	I/O	General purpose digital input/output
AIN5		AI	ADC input channel 5
QCD-	7	I/O	USB D- channel
QCD+	8	I/O	USB D+ channel
CC2	9	I/O	Type-C connector configuration channel 2
CC1	10	I/O	Type-C connector configuration channel 1
DISC_MON	11	AO	Type-C VBUS monitor with internal discharge FET
VBUS_CTRL	12	I/O	External MOSFET control
VDD	13	P	HV LDO output for digital and analog circuits
IS_P	14	AI	Positive input of a current sense amplifier for output current sensing
IS_N	15	AI	Negative input of a current sense amplifier for output current sensing
VSS	16	GND	Power supply ground

[3] Signal Types:
I = Input
O = Output
A = Analog signal
P = Power
GND = Ground

2.3 SNPD17332FJG

2.3.1 Pin Assignment

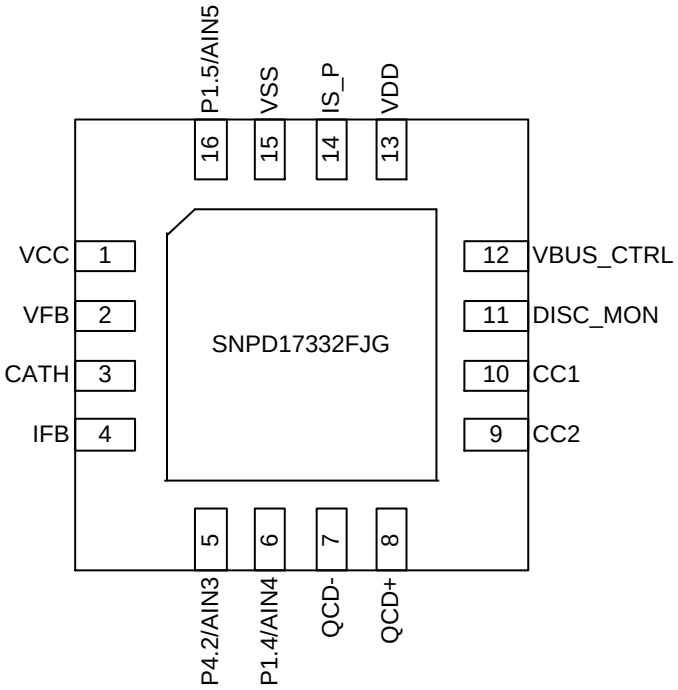


Figure 2–3 SNPD17332FJG Pin Assignment

2.3.2 Pin Description

Table 2–3 SNPD17332FJG Pin Description

Name	No.	Type[4]	Description
VCC	1	P	Power supply input voltage
VFB	2	AI	Feedback input for the constant-voltage loop
CATH	3	AI	Cathode of voltage regulation and compensation for other applications
IFB	4	AI	Feedback input for the constant-current loop
P4.2	5	I/O	General purpose digital input/output
AIN3		AI	ADC input channel 3
P1.4	6	I/O	General purpose digital input/output
AIN4		AI	ADC input channel 4
QCD-	7	I/O	USB D- channel
QCD+	8	I/O	USB D+ channel
CC2	9	I/O	Type-C connector configuration channel 2
CC1	10	I/O	Type-C connector configuration channel 1
DISC_MON	11	AO	Type-C VBUS monitor with internal discharge FET
VBUS_CTRL	12	I/O	External MOSFET control
VDD	13	P	HV LDO output for digital and analog circuits
IS_P	14	AI	Positive input of a current sense amplifier for output current sensing
VSS	15	GND	Power supply ground
P1.5	16	I/O	General purpose digital input/output
AIN5		AI	ADC input channel 5

[4] Signal Types:
I = Input
O = Output
A = Analog signal
P = Power
GND = Ground

2.4 SNPD1734HJG

2.4.1 Pin Assignment

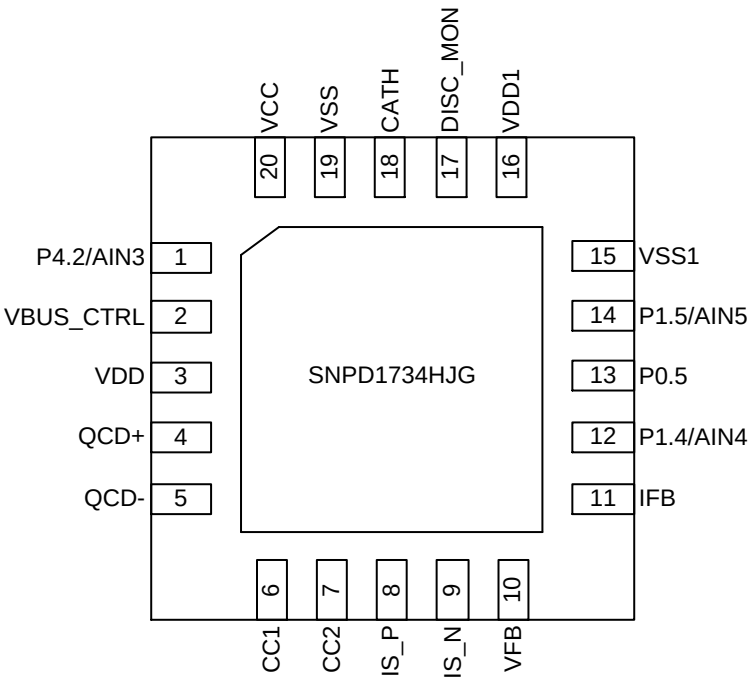


Figure 2–4 SNPD1734HJG Pin Assignment

2.4.2 Pin Description

Table 2–4 SNPD1734HJG Pin Description

Name	Pin No.	Type[5]	Description
P4.2	1	I/O	General purpose digital input/output
AIN3		AI	ADC input channel 3
VBUS_CTRL	2	I/O	External MOSFET control
VDD	3	P	HV LDO output for digital and analog circuits
QCD+	4	I/O	USB D+ channel
QCD-	5	I/O	USB D- channel
CC1	6	I/O	Type-C connector configuration channel 1
CC2	7	I/O	Type-C connector configuration channel 2
IS_P	8	AI	Positive input of a current sense amplifier for output current sensing
IS_N	9	AI	Negative input of a current sense amplifier for output current sensing
VFB	10	AI	Feedback input for the constant-voltage loop
IFB	11	AI	Feedback input for the constant-current loop
P1.4	12	I/O	General purpose digital input/output
AIN4		AI	ADC input channel 4
P0.5	13	I/O	General purpose digital input/output
P1.5	14	I/O	General purpose digital input/output
AIN5		AI	ADC input channel 5
VSS1	15	GND	Power supply ground
VDD1	16	P	HV LDO output for digital and analog circuits
DISC_MON	17	AO	Type-C VBUS monitor with internal discharge FET
CATH	18	AI	Cathode of voltage regulation and compensation for other applications
VSS	19	GND	Power supply ground
VCC	20	P	Power supply input voltage

[5] Signal Types:
I = Input
O = Output
A = Analog signal
P = Power
GND = Ground

3 System

3.1 MCU Subsystem

The SNPD1730 series has a MCU subsystem, which integrates an 8-bit 8051 processor. The MCU subsystem includes a 16 KB flash ROM, a 1.25 KB SRAM, and two 8-bit timers consisting of 32 MHz RC oscillators and 16 kHz RC oscillators to achieve high efficiency with low power consumption.

3.2 USB-PD Subsystem

3.2.1 USB-PD Physical Layer

The USB-PD physical layer consists of a transmitter and a receiver that communicate BMC-encoded data over the configuration channel (CC) based on the PD 3.1 standard. All communication is half-duplex. The physical layer or PHY provides collision avoidance to minimize communication errors on the channel.

The USB-PD block includes all termination resistors (R_P and R_D) and their switches as required by the USB-PD specification. R_P and R_D resistors are required to implement connection detection, plug orientation detection, and for establishing USB DFP/UFP roles. The R_P resistor is implemented as a current source.

According to the USB Type-C specification, a Type-C controller such as the SNPD1730 series must present certain termination resistors depending on its role in its unpowered state. The sink role in a power bank application requires R_D resistors to be present on the CC pins whereas the DFP role, as in a power adapter, requires both CC pins to be open. To be flexible for such applications, the SNPD1730 series includes the resistors required in the unpowered state on separate pads or pins.

3.2.2 ADC

The high precision 12-bit SAR ADC is used to detect and monitor analog signals of the peripherals such as the signals of the voltage detection circuit at CC1/CC2 and QCD+/QCD-, output voltage and current of VBUS, and internal thermal sensor and signals for external NTC thermal detection.

3.2.3 Charger Detection (QCD+/QCD-)

The D+/D- detection and charging protocol are compliant with conventional battery charging protocol (BC1.2) and Qualcomm Quick Charge 2.0/3.0/4.0/4.0+/5.0 charging protocols.

3.2.4 VBUS Overcurrent and Overvoltage Protection

The VBUS voltage sensing circuit and the shunt regulator of the SNPD1730 series form an integrated hardware protection circuit with fast response and adjustability for VBUS overvoltage and overcurrent protection.

3.2.5 Low-side Current Sense Amplifier (LSCSA)

The SNPD1730 series has a built-in current sensing circuit with input offset cancellation and programmable gain selections including 20, 40, 60, 80 and 100 V/V. With an external 5 mΩ precision resistor, the accuracy of the sensing circuit is 50 mA. The LSCSA also supports constant current mode in a power adapter application as a source.

3.2.6 MOSFET of Gate Driver on VBUS Path

A built-in gate driver controls the external MOS switch on the VBUS. The MOS switch is turned on when the Type-C sink side is attached. The MOS switch is turned off when the Type-C sink side is detached or an error (i.e. overcurrent, short circuit...) occurs.

3.2.7 VBUS Discharger FETs

The VBUS discharge circuit of the SNPD1730 series discharges secondary-side bulk capacitor voltage when a device is removed or during voltage decrease (i.e. from 20V to 12V) to achieve the time requirement of the USB-PD specification. The typical value of the sink current is 16 mA.

3.2.8 Shunt Regulator

Two regulators are parallel and connected to an open-drain output, CATH pin. The operation of each feedback loop is similar to that of a typical TL431 shunt regulator except that VCATH operating range is wider, from -0.3V to VCC + 0.3V, which enables simple designs of the converters with a wider output range.

The VFB DAC and IFB DAC convert the signals from the MCU subsystem to reference voltage and current (VREF_CV and VREF_CC) for the voltage and current feedback loops (VFB and IFB) respectively. The analog output range of the 11-bit DAC is from 0 to VDAC_MAX (typically 3V), which makes output voltage resolution as small as 10 mV, 14.6 mV, or 20 mV to achieve high-precision CV regulation.

3.3 Power System

The SNPD1730 series can operate from single external supply source, VCC (3.0V to 30V). When powered through VCC, the internal regulator generates a VDD of 5V for chip operation. The regulated supply is used directly inside some analog blocks. The SNPD1730 series has three different power modes: normal, idle, and stop. The POR (Power-on Reset) status is when power is valid and an internal reset source is asserted or the sleep controller is sequencing the system out of reset.

Transitions between these power modes are managed by the power system. When powered through the VCC pin, the VDD cannot be used to power external devices and should be connected to a 1 µF capacitor for regulator stability. These pins are not supported as power supplies. Figure 4–1 and Figure 4–2 show the application diagrams for capacitor connections.

Table 3–1 Power Mode

Name	Description
Normal Mode	Power is valid and the CPU is executing instructions.
Idle Mode	Power is valid and the CPU is not executing instructions. All logic that is not operating is clock gated to save power.
Stop Mode	The main regulator and most blocks are shut off. The stop regulator powers logic, but only the low-frequency clock is available.

4 Application – Power Adapter

The SNPD1730 series controls the power supply to the device according to the response of the device from the handshake when the power adapter, the device, and the AC power supply are connected. In the power converter application, the shunt regulator of the SNPD1730 series forms a feedback path with an optocoupler. The feedback voltage from the VCC divider voltage and the CATH signal are combined and transmitted to the voltage comparator of the shunt regulator through VFB to compare with VREF_CV from VFB DAC. The feedback current, IS_N and IS_P, from the low side current sense amplifier and the CATH signal are combined and transmitted to the voltage comparator of the shunt regulator through IFB to compare with VREF_CC from IFB DAC. The shunt regulator connects to CATH with optocoupler to feedback signals to the primary-side that has a converter, and to regulate the output voltage and current from the secondary-side where a device is connected depending on the feedback signals. When the power is supplied through VBUS, the SNPD1730 series precisely charges various devices using the USB-PD or the QC protocol. Figure 4–1 and Figure 4–2 illustrate power adapter application with PMOS and NMOS control respectively.

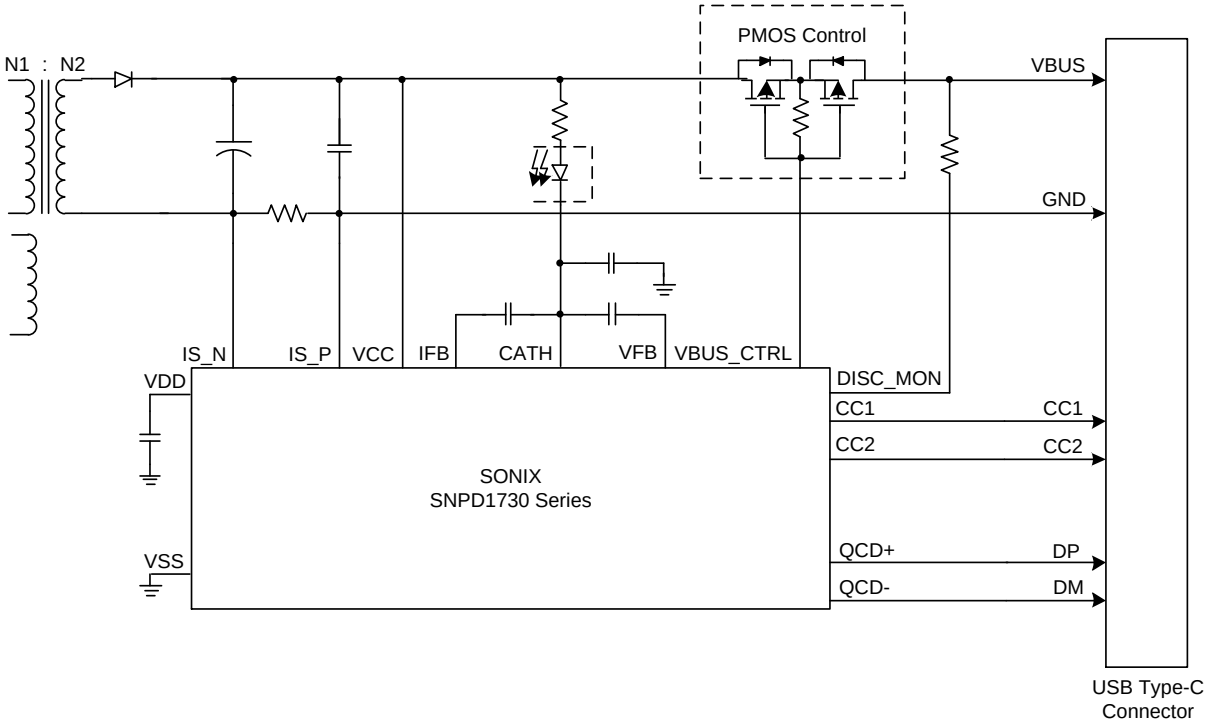


Figure 4–1 Power Adapter Application with PMOS Control

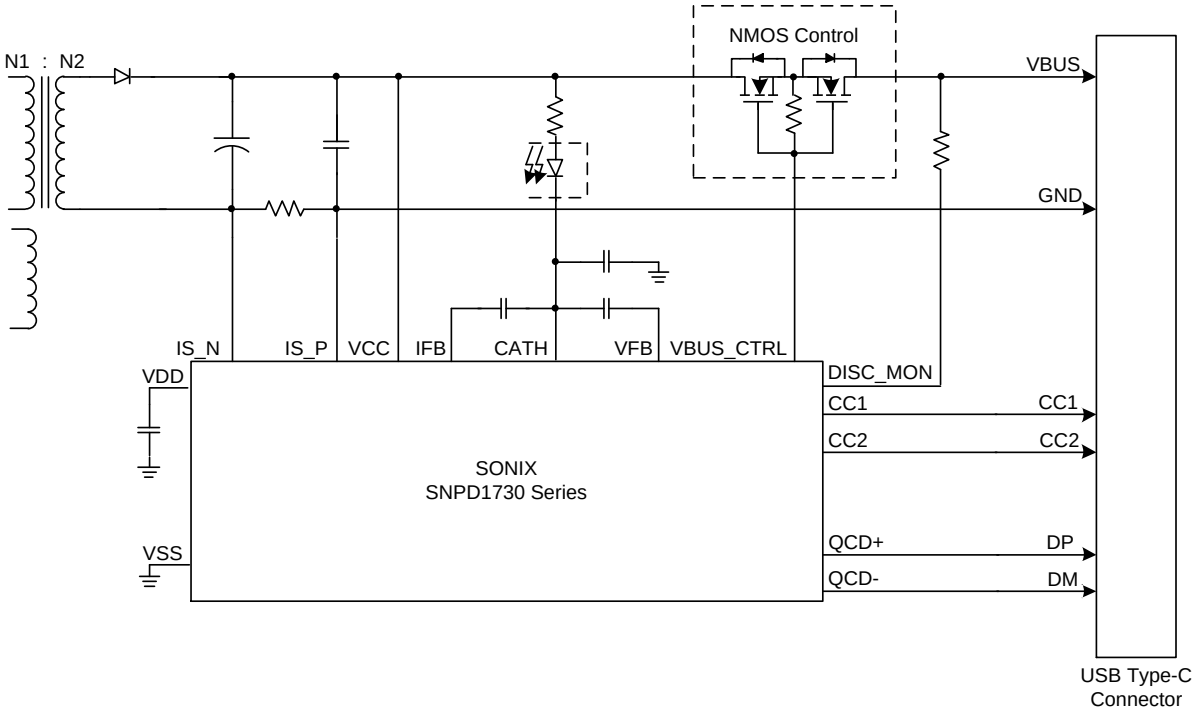


Figure 4–2 Power Adapter Application with NMOS Control

5 Device Operating Conditions

5.1 Absolute Maximum Ratings

Table 5–1 Absolute Maximum Ratings[6] [7] [8]

Parameter		Rating	Unit
Supply Voltage Ranges	VCC	-0.3 to 33	V
Input Voltage Ranges	CC1, CC2, QCD+, QCD-, VBUS_CTRL, DISC_MON, CATH	-0.3 to VCC + 0.3 (Max. 33V)	
	IS_P, IS_N, VFB, IFB, GPIO, ADC	-0.3 to 5.5	
Output Voltage Ranges	VBUS_CTRL	-0.3 to VCC + 8 (Max. 33V)	
	CC1, CC2, QCD+, QCD-, IS_P, IS_N, DISC_MON, GPIO, VDD	-0.3 to 5.5	
Ambient Temperature Ranges (T_A)		-40 to 105	°C
Operating Junction Temperature Ranges (T_J)		-40 to 105	
Storage Temperature Ranges (T_{STG})		-40 to 150	

5.2 Recommended Operating Conditions

Table 5–2 Recommended Operating Conditions

Parameter	MIN.	TYP.	MAX.	Unit
Supply Voltage, VCC	3.0	–	30	V
Supply Ground, Thermal Pad	0	0	0	

Table 5–3 Electrical Characteristics for DC Specifications

Parameter		Conditions	MIN.	TYP.	MAX.	Unit
Input Voltage	V_{CC}	–	3.0	–	30	V
Output Voltage	V_{DD}	V_{CC} > 5.4V	4.8	5.0	5.2	
Input Capacitance	C_{VCC}	–	–	1	–	µF
Output Capacitance for VDD	C_{VDD}	–	–	1	–	
Supply Current for VCC	I_{VCC}	–	–	–	20	mA
VCC Power Consumption in the Normal Mode	I_{VCC_A}	V_{CC} = 5V, T_A = 25°C, CC1/CC2 in Tx or Rx, no I/O sourcing current, QCD+/QCD- output voltage, HVLDO/Shunt Regulator/DAC/ LSCSA/NMOS Gate Driver/ADC on, CPU at 8 MHz	–	6	–	

[6] Long-term exposure to absolute maximum ratings may affect device reliability, and permanent damage may occur if the operation exceeds the maximum ratings.
[7] All voltage values are with respect to VSS.
[8] The ratings are measured based on reference design.

Parameter		Conditions	MIN.	TYP.	MAX.	Unit
VCC Power Consumption in the Idle Mode	I_{VCC_S}	V_{CC} = 5V, T_A = 25°C, all blocks sleep except for CPU, CC/QCD+/QCD-, and Shunt Regulator/DAC/ LSCSA/ADC on	–	2	–	mA
VCC Power Consumption in the Stop Mode	I_{VCC_DS}	V_{CC} = 5V, T_A = 25°C, Type-C not attached. CC/QCD+/QCD- attach function enabled for wakeup	–	450	–	μA

Table 5–4 Electrical Characteristics for I/O DC Specifications[9]

Parameter		Conditions	MIN.	TYP.	MAX.	Unit
Input Voltage HIGH Threshold	V_{IH}	–	0.7 x V_{DD}	–	V_{DD}	V
Input Voltage LOW Threshold	V_{IL}	–	V_{ss}	–	0.3 x V_{DD}	
Output Voltage HIGH Threshold	V_{OH}	–	V_{DD} - 0.5	–	–	
Output Voltage LOW Threshold	V_{OL}	–	–	–	V_{SS} + 0.5	
Internal Pull-up Resistance	R_{PU}	V_{DD} = 5V	–	50	–	kΩ
Output Source Current	I_{OH}	V_{OP} = V_{DD} - 0.5V	–	10	–	mA
Output Sink Current	I_{OL}	V_{OP} = V_{SS} + 0.5V	–	10	–	
Input Leakage Current	I_{LC}	–	–	–	2.0	μA
VCONN Output Voltage Threshold	V_{CONN}	–	V_{DD} - 0.5V	–	–	V
VCONN Output Current Threshold	I_{CONN}	–	–	–	20	mA

Table 5–5 Electrical Characteristics for ADC DC Specifications

Parameter		Conditions	MIN.	TYP.	MAX.	Unit
ADC Reference Voltage	V_{ADC_REF}	–	2.0	–	V_{DD}	V
ADC Clock Frequency	F_{ADCCLK}	–	–	–	12	MHz
ADC Sampling Rate	F_{ADCSMP}	V_{DD} = 5V	–	–	200	kHz
ADC Offset Voltage	V_{ADC_Offset}	–	-5.0	–	5.0	mV
No Missing Code	NMC	–	10	–	12	Bits

Table 5–6 Electrical Characteristics for Current Sense Amplifier

Parameter		Conditions	MIN.	TYP.	MAX.	Unit
CSA Accuracy	V_{CM_ACC1}	5 mV < Vsense < 10 mV	-15	–	15	%
	V_{CM_ACC2}	10 mV < Vsense < 15 mV	-10	–	10	
	V_{CM_ACC3}	15 mV < Vsense < 20 mV	-6.0	–	6.0	
Register-programmable Current Sense Voltage Gain	G_{vv}	+20/Step	20	–	100	V/V
Unit Gain Bandwidth	U_{BW}	–	–	250	–	kHz

[9] The parameters below apply to P0.5, P1.4, P1.5, and P4.2.

Table 5–7 Electrical Characteristics for DISC_MON

Parameter		Conditions	MIN.	TYP.	MAX.	Unit
VBUS Discharger Sinking Current	I_{DISC_MON}	V_{DISC_MON} = 20V	–	16	–	mA

Table 5–8 Electrical Characteristics for VCC_DISC

Parameter		Conditions	MIN.	TYP.	MAX.	Unit
VCC Discharger Sinking Current	I_{VCC_DISC1}	V_{CC} = 20V	–	20	–	mA
	I_{VCC_DISC2}		–	40	–	
	I_{VCC_DISC3}		–	60	–	
	I_{VCC_DISC4}		–	80	–	
	I_{VCC_DISC5}		–	100	–	
	I_{VCC_DISC6}		–	120	–	

Table 5–9 Electrical Characteristics for QCD+/QCD- Specifications

Parameter		Conditions	MIN.	TYP.	MAX.	Unit
QCD+ Pull-down Resistance	R_{L_D+}	–	300	–	1500	kΩ
QCD- Pull-down Resistance	R_{L_D-}	–	14.25	–	24.80	
Register-programmable Output High Voltage	$V_{OH\_3.0V}$	–	2.70	3.00	3.30	V
	$V_{OH\_1.8V}$	–	1.62	1.80	1.98	
	$V_{OH\_0.6V}$	–	0.5	0.60	0.7	
	V_{OH_APPLE}	Apple 2.4A mode	2.43	2.70	2.97	
Register-programmable Input Trip Voltage	V_{IH_D+D-}	–	1.90	2.00	2.10	
		–	0.90	1.00	1.10	
		–	0.25	0.325	0.40	
QCD+/QCD- Switch On-Resistance	R_{ON_D+D-}	–	–	20	40	Ω
Output Low Voltage	V_{OL_3V}	R_{LOAD} = 6 kΩ	–	–	0.20	V
	$V_{OL\_1.8V}$					
	$V_{OL\_0.6V}$					

Table 5–10 Electrical Characteristics for CC1/CC2 Specifications

Parameter		Conditions	MIN.	TYP.	MAX.	Unit
Output High Voltage	V_{OH}	–	1.04	–	1.20	V
Output Low Voltage	V_{OL}	–	-0.075	–	0.075	
Rise Time/Fall Time	T_{RISE}/T_{FALL}	–	300	–	675	ns
DFP CC Termination for Default USB Power	$I_{CC\_default}$	–	68	80	92	µA
DFP CC Termination for 1.5A power	$I_{CC\_1.5A}$	–	165	180	194	
DFP CC Termination for 3.0A power	I_{CC_3A}	–	303	330	356	
UFP CC Termination	Rd	–	4.59	5.10	5.61	kΩ
Power Cable Termination	Ra	–	800	1000	1200	Ω

Table 5–11 Electrical Characteristics for Shunt Regulator Specifications

Parameter		Conditions	MIN.	TYP.	MAX.	Unit
Off-State CATH Current	I_{CATH_OFF}	Open-circuited CATH pin	–	–	2.0	µA
Maximum CATH Sinking Current	I_{CATH_MAX}	–	2.0	–	20	mA

Table 5–12 Electrical Characteristics for Gate Driver Specifications

Parameter		Conditions	MIN.	TYP.	MAX.	Unit
Gate to Source voltage driving external FETs	V_{GS}	–	4.5	–	8	V
Resistance when pull-down enable	R_{PD}	–	–	–	4	kΩ

5.3 AC Characteristics

Table 5–13 AC Specifications

Parameter		Conditions	MIN.	TYP.	MAX.	Unit
Main oscillator frequency	F_{CPU}	–	–	–	32	MHz
Low frequency oscillator	F_{ILRC}	–	–	16	–	kHz
Wakeup from idle mode	T_{IDLE}	–	–	180	–	μs
Wakeup from stop mode	T_{STOP}	–	–	350	–	
Power-on I/O Initialization Time	T_{POR}	–	–	6.25	–	ms

6 Mechanical Data

6.1 Thermal Data

The permissible operating temperature range for the bearing is -40°C to 105°C.

6.2 Package Information

6.2.1 Nomenclature

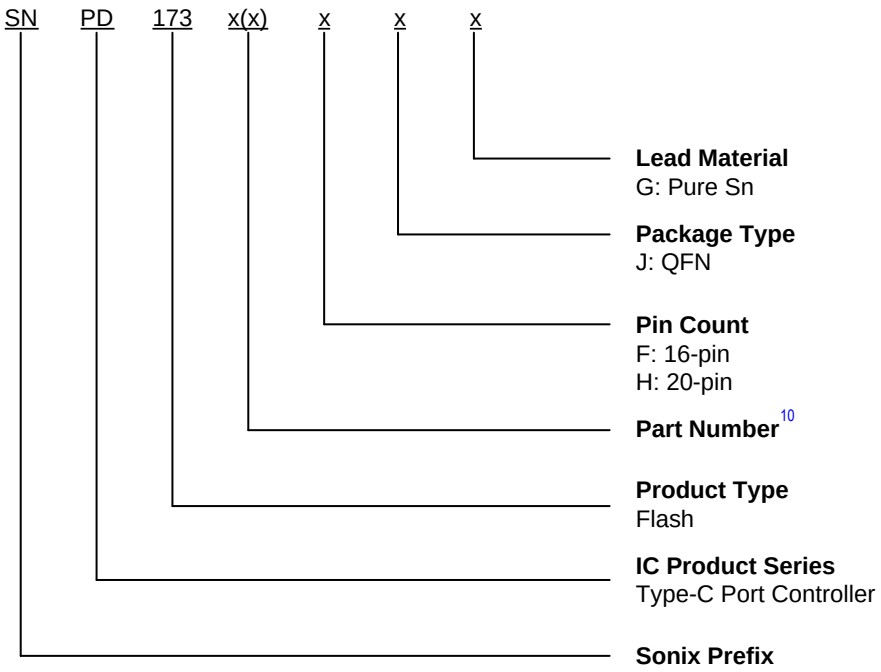


Figure 6–1 Device Nomenclature

[10] For details, refer to 1.3 Selection Table.

6.2.2 Marking

The product ID and symbols shown in the figure below represents an example and may vary according to different packages.

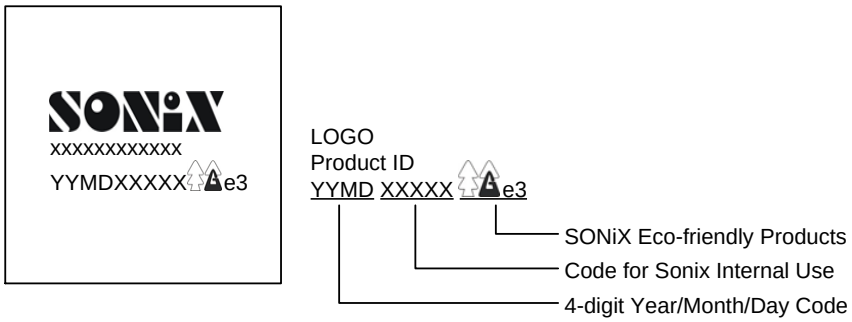
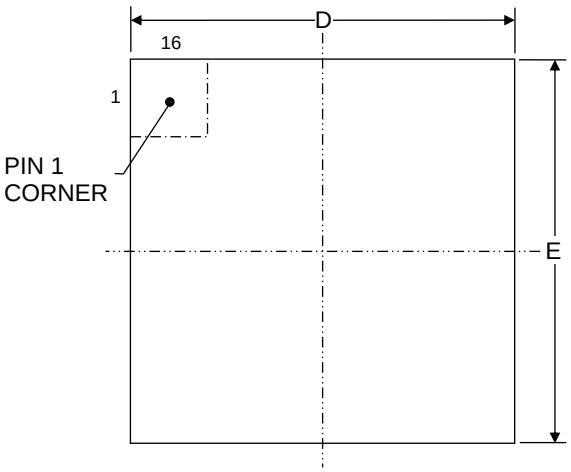


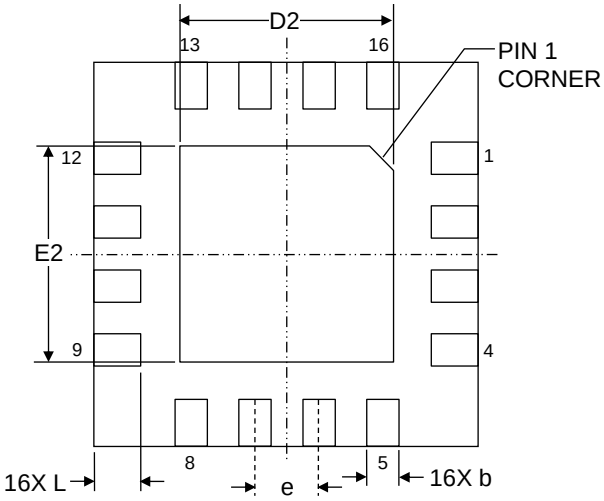
Figure 6–2 Example of Device Marking

6.2.3 Package Dimensions

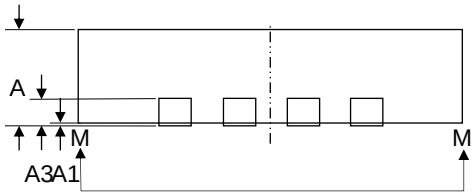
I. QFN16L (4 x 4 x 0.8 mm, Pitch: 0.65 mm)



TOP VIEW



BOTTOM VIEW
VIEW M－M

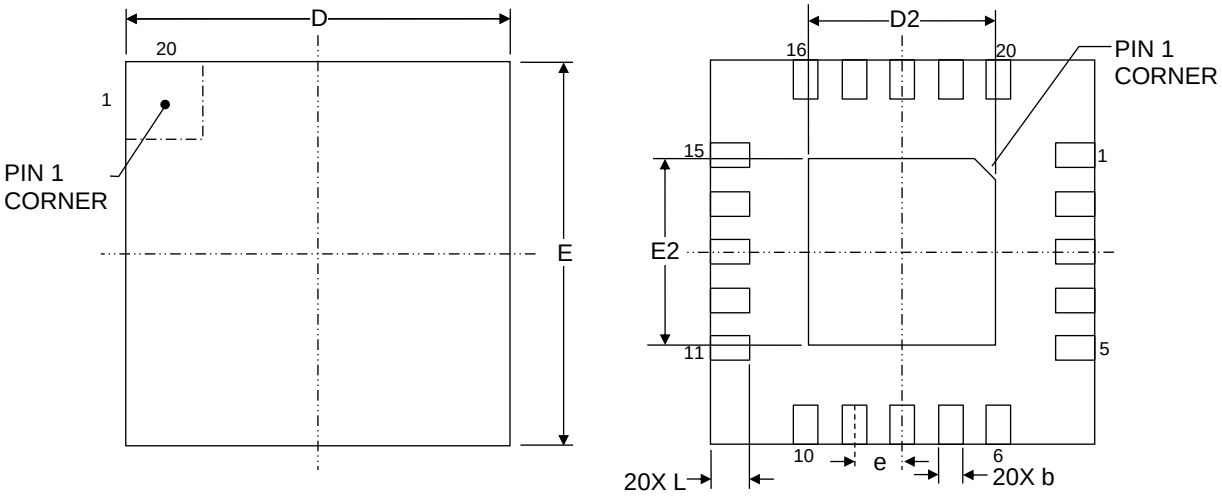


SIDE VIEW

Symbols	Dimension in mm[11]			Dimension in inch		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.80	0.90	0.028	0.031	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3		0.20 REF			0.008 REF	
b	0.25	0.30	0.35	0.010	0.011	0.012
D		4.00 BSC			0.157 BSC	
E		4.00 BSC			0.157 BSC	
e		0.65 BSC			0.025 BSC	
D2	2.00	2.40	2.80	0.078	0.094	0.110
E2	2.00	2.40	2.80	0.078	0.094	0.110
L	0.30	0.40	0.50	0.011	0.015	0.019

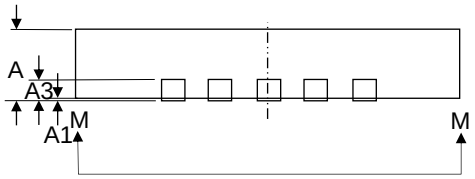
[11] Controlling dimension: millimeter (mm)

II. QFN20L (4 x 4 x 0.8 mm, Pitch: 0.5 mm)



TOP VIEW

BOTTOM VIEW
VIEW M－M



SIDE VIEW

Symbols	Dimension in mm[12]			Dimension in inch		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.80	0.90	0.028	0.031	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3		0.20 REF			0.008 REF	
b	0.18	0.24	0.30	0.007	0.010	0.012
D		4.00 BSC			0.157 BSC	
E		4.00 BSC			0.157 BSC	
e		0.50 BSC			0.020 BSC	
D2	1.90	2.30	2.70	0.075	0.090	0.106
E2	1.90	2.30	2.70	0.075	0.090	0.106
L	0.30	0.40	0.50	0.012	0.016	0.020

[12] Controlling dimension: millimeter (mm)

6.3 Packing Appearance and Storage Information

6.3.1 Packing Quantity Information

Table 6–1 Packing Quantity Information

Type	Pin Count	Carry Type	Package Size	IC Q'ty per Tube or Tray or Reel	Tube or Tray or Reel Q'ty per Inner Box	Total Q'ty in One Inner Box	Inner Box Q'ty per Carton	IC Q'ty per Carton
QFN	16	Tray	4 x 4	490	10	4900	6	29400
QFN	16	Tape & Reel	4 x 4	2500	1	2500	10	25000
QFN	20	Tray	4 x 4	490	10	4900	6	29400
QFN	20	Tape & Reel	4 x 4	2500	1	2500	10	25000

6.3.2 Packing Box/Carton Dimension

Table 6–2 Inner Box/Carton Dimension

Inner Box/Carton	Carry Type	Dimension in mm
Inner Box	Tray	358 x 159 x 88
	Tube	610 x 170 x 100
	Tape & Reel	355 x 340 x 50
Carton	Tray	555 x 435 x 280
	Tube	630 x 360 x 345
	Tape & Reel	560 x 360 x 385

6.3.3 Temperature and Humidity Environmental Control Requirements in Storage

Table 6–3 Store Condition

Control Requirement	Specification
Temp. (°C)	24 ± 6
Humid. (%RH)	60 ± 20

6.3.4 Shelf-life

1. The shelf life for unopened vacuum pack products is four years after the date on the label.
2. Once the packaging is opened the product should be conducted SMT process within 168 hours and environmental control is under ≤ 30°C / 60 %RH.
3. If the product has been exposed to the room environment for more than 168 hours, it should be baked in an oven at 125°C for 10 hours and vacuum packed.

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